AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A logic circuit, comprising:

a first logic stage comprising first logic circuitry operable to receive a first set of input signals and to generate a first output signal in response thereto, wherein said first logic circuitry comprises clocked precharge and evaluate transistors and further comprises full-complementary low-beta-ratio static logic; and

at least one subsequent logic stage, comprising second logic circuitry operable to receive a second set of input signals and to generate a second output signal in response thereto, wherein said second logic circuitry comprises non-clocked, low-beta-ratio static logic.

2. (Previously Presented) The logic circuit of claim 1, wherein said first logic circuitry comprises a plurality of input transistors configured in a first tapered stack.

3. (Previously Presented) The logic circuit of claim 2, wherein said clocked precharge circuitry comprises at least one pMOS transistor operable to hold a first node at a voltage, Vdd, during a precharge phase.

4. (Previously Presented) The logic circuit of claim 3, wherein said tapered stack of input transistors comprises a plurality of nMOS transistors operable to conditionally pull said first node to a lower voltage during an evaluation phase in response to a predetermined set of input signals.

5. (Previously Presented) The logic circuit of claim 4, wherein said subsequent logic stage comprises a plurality of input transistors configured in a second tapered stack connected to a second node that is maintained at a voltage, Vdd, during a precharge phase and wherein said input transistors are operable to conditionally pull said node to a lower voltage during an evaluation phase in response to a predetermined set of input signals.

6. (Previously Presented) The logic circuit of claim 5, wherein said low-beta-ratio static logic in said second logic circuitry comprises a plurality of pMOS transistors operably connected to said second node and wherein said plurality of pMOS transistors are operable to hold said second node at a voltage, Vdd, during said precharge phase.

7. (Previously Presented) The logic circuit of claim 6, wherein said second tapered stack of input transistors comprises a plurality of nMOS transistors with each individual nMOS transistor in said second stack has its gate connected to the gate of one of said plurality of pMOS transistors.

8. (Previously Presented) The logic circuit of claim 7, wherein the beta-ratio of said non-clocked static logic in said second logic circuitry is less than 1:1.

9. (Previously Presented) The logic circuit of claim 8, wherein the precharge load for maintaining said second node at Vdd is distributed across said plurality of pMOS transistors connected to said second node.

10. (Previously Presented) A method of operating a logic circuit, comprising:

receiving a first set of input signals in a first logic circuit and generating a first output signal in response thereto,

receiving a second set of input signals in a second logic circuit and generating a second output signal in response thereto,

wherein said first logic circuitry comprises clocked precharge and evaluate transistors and further comprises full-complementary low-beta-ratio static logic; and

wherein said second logic circuitry comprises non-clocked, low-beta-ratio static logic.

11. (Previously Presented) The method of claim 10, wherein said first logic circuitry comprises a plurality of input transistors configured in a first tapered stack.

12. (Previously Presented) The method of claim 11, wherein said clocked precharge circuitry comprises at least one pMOS transistor operable to hold a first node at a voltage, Vdd, during a precharge phase.

13. (Previously Presented) The method of claim 12, wherein said tapered stack of input transistors comprises a plurality of nMOS transistors operable to conditionally pull said first node to a lower voltage during an evaluation phase in response to a predetermined set of input signals.

14. (Previously Presented) The method of claim 13, wherein said subsequent logic stage comprises a plurality of input transistors configured in a second tapered stack and wherein said second tapered stack of input transistors is connected to a second node that is maintained at a voltage, Vdd, during a precharge phase and wherein said input transistors are operable to conditionally pull said node to a lower voltage during an evaluation phase in response to a predetermined set of input signals.

15. (Previously Presented) The method of claim 14, wherein said low-beta-ratio static logic in said second logic circuitry comprises a plurality of pMOS transistors connected to said second node and wherein said plurality of pMOS transistors are operable to hold said second node at a voltage, Vdd, during said precharge phase.

16. (Previously Presented) The method of claim 15, wherein said second tapered stack of input transistors comprises a plurality of nMOS transistors with each individual nMOS transistor in said second stack has its gate connected to the gate of one of said plurality of pMOS transistors.

17. (Previously Presented) The method of claim 16, wherein the beta-ratio of said non-clocked static logic in said second logic circuitry is less than 1:1.

18. (Previously Presented) The method of claim 17, wherein the input transistors in said second tapered stack in said second logic circuitry, wherein said clocked precharge circuitry comprises at least one pMOS transistor operable to hold a first node at a voltage, Vdd, during an evaluation phase.